

*Citation for published version:*

Qi, W, Li, S, Yuan, H, Tan, SC & Hui, SYR 2019, 'High-Power-Density Single-Phase Three-Level Flying-Capacitor Buck PFC Rectifier', *IEEE Transactions on Power Electronics*, vol. 34, no. 11, 8630661, pp. 10833-10844. <https://doi.org/10.1109/TPEL.2019.2896585>

*DOI:*

[10.1109/TPEL.2019.2896585](https://doi.org/10.1109/TPEL.2019.2896585)

*Publication date:*

2019

*Document Version*

Peer reviewed version

[Link to publication](#)

© 2019 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other users, including reprinting/ republishing this material for advertising or promotional purposes, creating new collective works for resale or redistribution to servers or lists, or reuse of any copyrighted components of this work in other works.

**University of Bath**

## **Alternative formats**

If you require this document in an alternative format, please contact:  
[openaccess@bath.ac.uk](mailto:openaccess@bath.ac.uk)

### **General rights**

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

### **Take down policy**

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

# High-Power-Density Single-Phase Three-Level Flying-Capacitor Buck PFC Rectifier

Wenlong Qi, *Student Member, IEEE*, Sinan Li, *Member, IEEE*, Huawei Yuan, *Member, IEEE*, Siew-Chong Tan, *Senior Member, IEEE* and S. Y. (Ron) Hui, *Fellow, IEEE*

*Abstract*— Active pulsating-power-buffering (PPB) is an effective technique to reduce the energy storage requirement of a single-phase power-factor-correction (PFC) rectifier. Existing single-phase solutions with active PPB, however, generally suffer from high voltage stresses, leading to increased power losses as well as the need for high-voltage-rating semiconductor switches. Previous works have been focusing on two-level switching converter configurations, and thus have failed to address the high-voltage-stress problem. In this paper, a single-phase three-level flying-capacitor PFC rectifier with PPB embedded switching is proposed. The flying capacitor not only clamps the voltage stresses of all power devices but also functions as a PPB capacitor. The operating principles, control methods, and design guidelines are detailed and the feasibility of the proposed converter is verified through a 48-W (48-V/1-A) hardware prototype. The proposed rectifier is shown to achieve nearly 50% reduction of the voltage stresses, 72% reduction of the buffering capacitor's volume and 23.8% reduction of the magnetic core size, as compared to a state-of-the-art two-level solution recently proposed. This new approach of formulating single-phase PFC rectifiers with active PPB could dramatically boost the system's efficiency and power density whilst reducing cost.

*Index Terms*—buck PFC rectifier, active power decoupling, three-level flying capacitor, automatic power decoupling.

## I. INTRODUCTION

Single-phase power-factor-correction (PFC) rectifiers with simultaneous high power-density, high conversion efficiency and high reliability ( $H^3$ ) are particularly desirable in many emerging applications such as LED driving (which requires a long service lifetime and a small form factor) [1]–[6] and quick charging for mobile phones (which demands a portable design and a high power efficiency) [7]–[9]. One critical challenge for conventional single-phase PFC rectifiers towards achieving  $H^3$  is the use of electrolytic

capacitors (E-caps) which are employed for buffering the double-line-frequency pulsing ripple power inherent in single-phase PFC rectifiers [10]–[14] (see  $C_b$  in Fig. 1(a)). On one hand, E-caps are known to have a relatively short lifetime (e.g. <7,000 hours at 105 °C) [15]. On the other hand, conventional single-phase rectifiers employing a two-port configuration (an ac port and a dc port) dictate a significant amount of energy storage capacity in  $C_b$  due to stringent dc-link voltage ripple requirement, thereby significantly increasing the overall volume of the system. The use of state-of-the-art semiconductor technology such as SiC and GaN can dramatically boost the system performance in terms of conversion efficiency and power density, However, as pointed out in [16], the use of ideal switch is not enough, and that further improvement is essentially attributed to advancement in passive components. In response to this developing trend, new derivatives of single-phase PFC rectifiers with a three-port architecture have been developed (see Fig. 1(b)). In this configuration,  $C_b$  is attached to a third ripple port, thus having the freedom to perform large voltage fluctuation (see  $\Delta v_c$ ). As the power of  $C_b$  is proportional to  $\Delta v_c$ , only a small  $C_b$  is needed to buffer the ripple power given a large  $\Delta v_c$ . Consequently, non-electrolytic capacitors such as film or laminated ceramic capacitors which are more reliable and compact can be adopted for  $C_b$  in this three-port configuration [17]. In literature, the methods of augmenting a third ripple port are referred to as active pulsating power buffering (PPB).

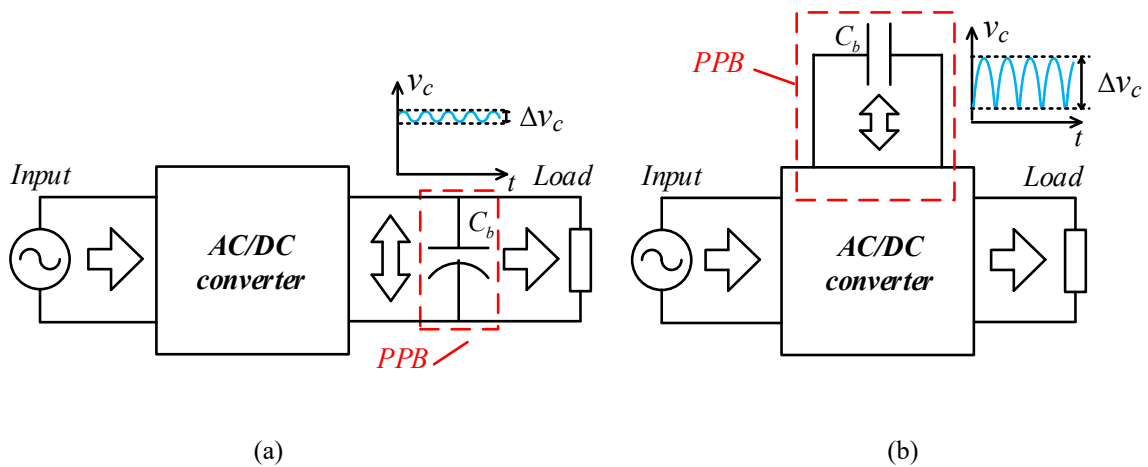


Fig. 1. Power conversion architecture of (a) conventional single-phase power converter with passive PPB and (b) three-port architecture with active PPB.

One simple means to achieving active PPB is to directly connect a bidirectional dc active filter in parallel (or series) to the dc-link [18]–[21]. Despite the effectiveness of energy reduction in  $C_b$ , the need for extra power electronics to construct a dc active filter compromises the effectiveness of volume reduction. In [22]–[25] the authors reported an integrated solution requiring no extra active switches for achieving active PPB, by sharing the use of active switches between a PFC rectifier and an active dc filter. Recently, a new concept called PPB embedded switching is further investigated which can reduce the number of both active and passive components [26]–[29]. With this concept, extra switching states (i.e., a capacitor charging state and a discharging state) are deliberately introduced into each switching cycle of the original PFC rectifier to perform active PPB, thereby avoiding the use of extra dc active filters. While rectifiers employing PPB embedded switching seem to have a great potential of achieving the ultimate goal of  $H^3$  single-phase power conversion, existing solutions are subjected to issues of high voltage stresses. In most of the solutions reported, the active switches and the diodes must withstand a peak voltage stress up to  $V_{ac}+V_{dc}$ , where  $V_{ac}$  is the peak ac voltage and  $V_{dc}$  is the output voltage, leading to high switching and conduction losses as well as the mandatory use of high-voltage rating semiconductors which are generally expensive. In [30], a three-level flying-capacitor buck-boost PFC rectifier is reported achieving low voltage stress, however, a limitation of the circuit is its output voltage must be higher than  $V_{ac}/2$ . In [31], a three-level flying-capacitor inverter is also reported with low voltage stress, however the double-line frequency ripple power can't be totally buffered by flying capacitor in this inverter.

In this paper, a high-power density and low-voltage-stress buck PFC rectifier is proposed to overcome the drawbacks of previous solutions. In particular, the typical three-level flying-capacitor rectifier topology and the PPB embedded switching concept are the fundamental building blocks for the proposed solution. **The fundamental concept behind the proposed rectifier is inspired by the work of [14] and [26].** The proposed rectifier enjoys all the benefits of a typical multi-level converter such as low voltage stresses and reduced magnetics usage. Additionally, no E-cap is needed as active PPB is embedded. The operating principles,

control method and design considerations of the rectifier are detailed in Section II to IV. As a benchmark, a comparison is also conducted in Section IV between the proposed PFC rectifier and the conventional buck PFC rectifier. The feasibility of the proposed E-cap-less three-level PFC rectifier is experimentally illustrated for a 48-W prototype. Section V provides a description of the experimental work, and a discussion on both the steady-state and the transient performances. Finally, Section VI gives the conclusions of the paper.

## II. SINGLE-PHASE THREE-LEVEL FLYING-CAPACITOR BUCK PFC RECTIFIER

### A. Circuit Configuration

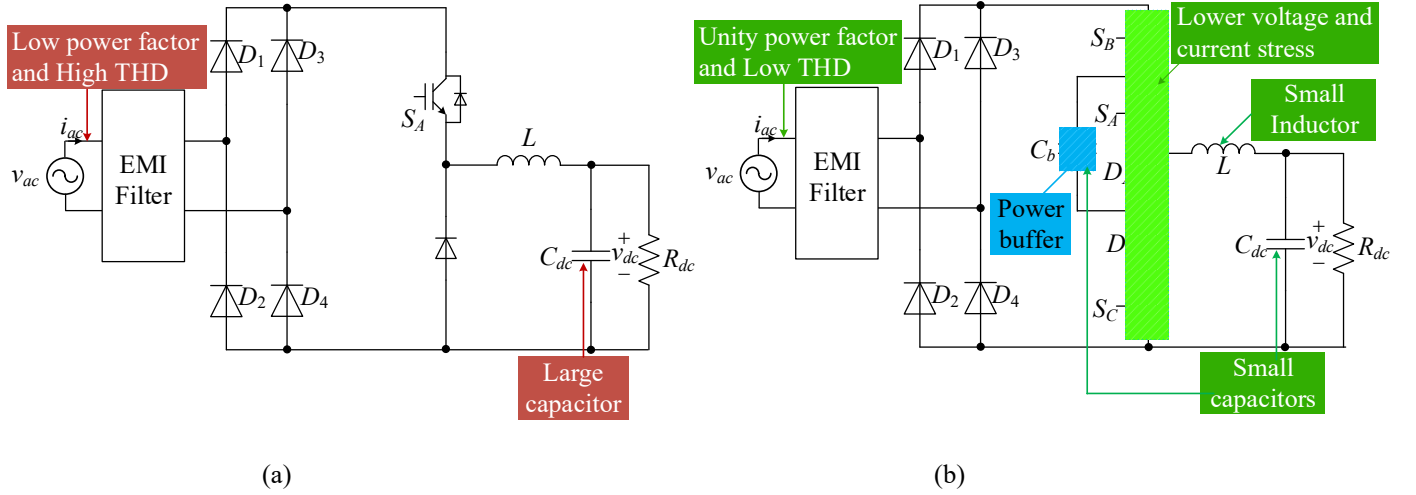


Fig. 2. Circuit diagrams of (a) conventional buck PFC rectifier and (b) the proposed three-level flying-capacitor buck PFC rectifier.

Fig. 2 (a) and (b) respectively illustrates the conventional buck PFC rectifier and the proposed three-level flying-capacitor buck PFC rectifier. Compared to the conventional solution, the proposed rectifier is augmented with two active switches ( $S_B, S_C$ ), one diode ( $D_C$ ) and one capacitor  $C_b$ . It can be observed that the topology of the proposed rectifier resembles that of a typical three-level flying-capacitor rectifier, except that an extra active switch  $S_C$  is needed, and that  $C_b$ ,  $C_{dc}$ , and  $L$  are much smaller. As will be explained in Section II-B, the addition of these extra power components results in the following key advantages over conventional buck PFC rectifier:

- (i) reduced volume of  $C_b$ , due to the active PPB function;

(ii) unity power factor and low THD, due to the controllability of the input current throughout the line period;

(iii) reduced voltage and current stress of all switching devices;

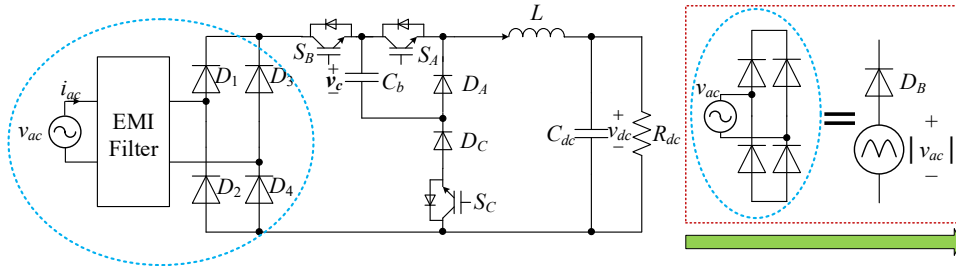
(iv) reduced volume of  $L$ , due to the reduced peak inductor current.

### B. Operating Principles

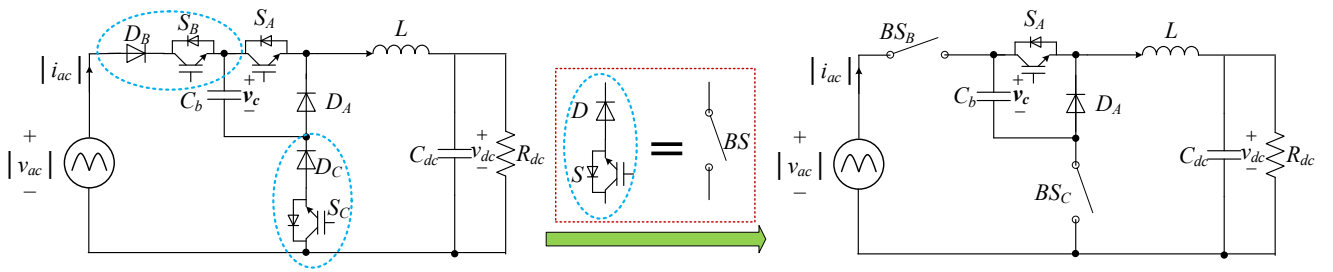
To simplify the analysis, the circuit topology in Fig. 2(c) is equivalently transformed into Fig. 3(c) following a two-step procedure as below:

Step 1 is to neglect the electromagnetic interference (EMI) filter and to represent the line voltage  $v_{ac}$  and the front-end diode bridge rectifier by a rectified sinusoidal voltage source  $|v_{ac}|$  that is in series with a diode  $D_B$  (from Fig. 3(a) to (b));

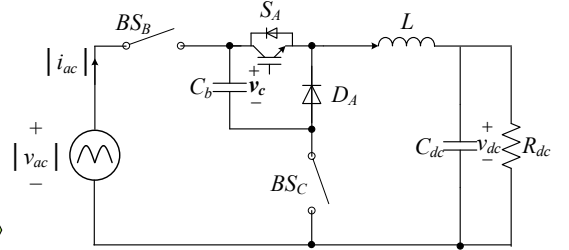
Step 2 is to replace any series connections of an MOSFET ( $S$ ) and a diode ( $D$ ) using a bi-quadrant switch ( $BS$ ) that can only conduct a positive current whilst blocking voltage bi-directionally (from Fig. 3(b) to (c)).



(a)



(b)



(c)

Fig. 3. Equivalent circuits of the proposed PFC rectifier.

In Fig. 3(c), the bi-quadrant switches  $BS_B$  and  $BS_C$  are switched complementarily. Assuming a continuous-conduction-mode (CCM) of operation, the rectifier has four switching states as depicted in Fig. 4. In *State 1* and *State 2*, the inductor is energized by  $|v_{ac}|$  and de-energized to the load, respectively, while  $C_b$  is not involved in circuit operation. These two switching states are identical to those of a buck converter; In *State 3* and *State 4*,  $C_b$  is part of the power flow path. Specifically,  $C_b$  is discharged by a current equivalent to the inductor current  $i_L$  in *State 3* and charged by a current equivalent to  $i_L$  in *State 4*. Thus, an extra capacitor charging state and a discharging state are created. By controlling the duration of *State 3* and *State 4*, the amount of power flowing into/out of  $C_b$  can be actively controlled, thereby achieving active PPB. Furthermore, the line current  $|i_{ac}|$  is always controllable irrespective of the line voltage level. This is because  $|i_{ac}|$  equals to  $i_L$  whenever  $BS_B=1$  (*State 1* and *State 4*), while it equals to 0 when  $BS_B=0$  (*State 2* and *State 3*). In contrast,  $|i_{ac}|$  cannot be controlled when  $|v_{ac}| < V_{dc}$  in the conventional buck PFC rectifier. Moreover, an additional feature is that the voltage ratings of  $S_A$  and  $D_A$  are always clamped by  $v_c$  which can be designed at a low voltage level (as will be explained in Section IV), while those of  $S_B$ ,  $S_C$ , and  $D_C$  are also de-rated due to the series insertion of  $C_b$  in the power flow path. A summary of the switching states are tabulated in Table I.

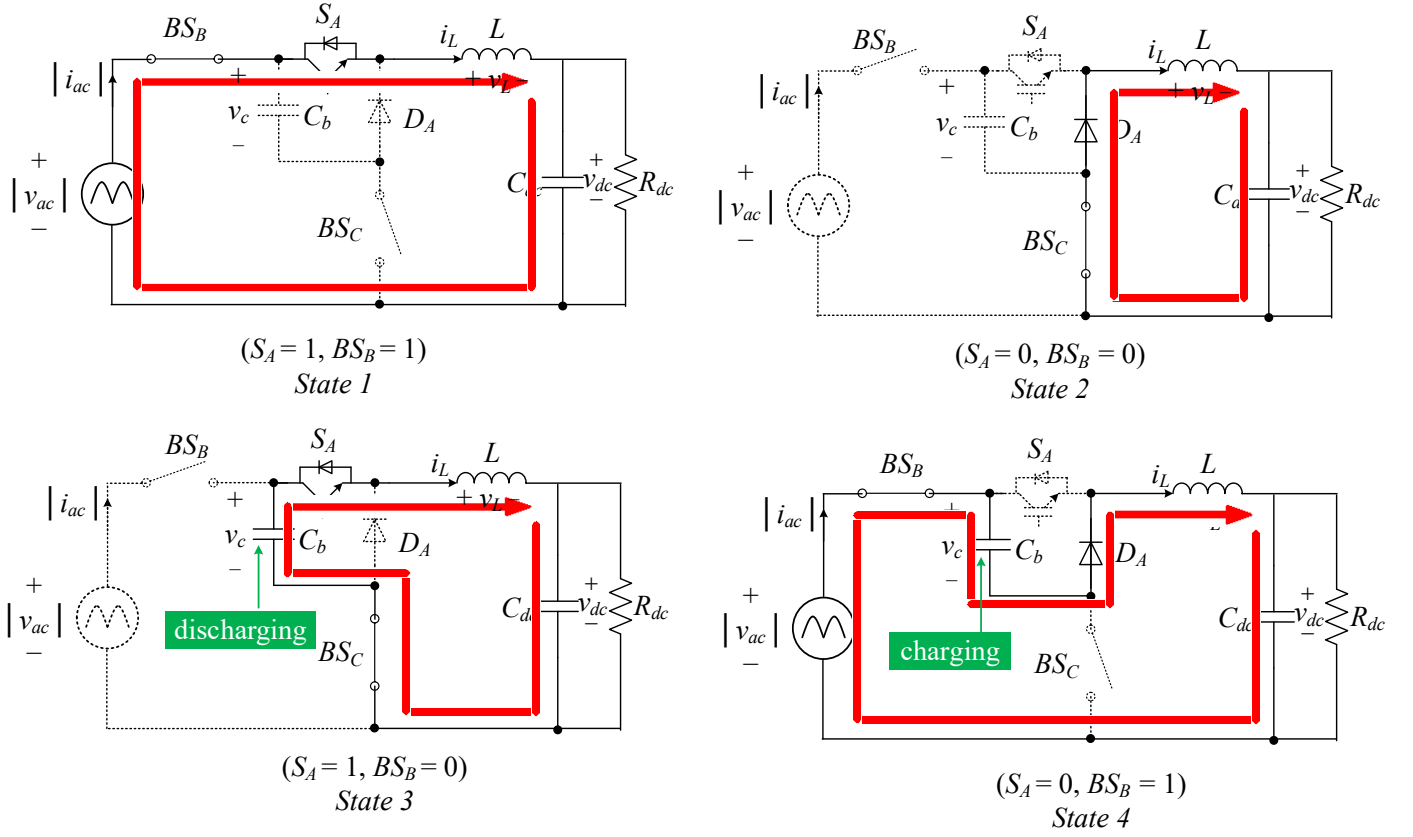


Fig. 4. Equivalent circuits of the proposed rectifier operating in State 1–State 4.

Table I. Summary of Switching States.

Operating State	$S_A$	$BS_B$	$C_b$	$v_L$
State 1	1	1	Idle	$ v_{ac}  - v_{dc}$
State 2	0	0	Idle	$-v_{dc}$
State 3	1	0	Discharge	$v_c - v_{dc}$
State 4	0	1	Charge	$ v_{ac}  - v_c - v_{dc}$

### C. Steady-State Circuit Analysis

Assuming a unity power factor and that  $v_{ac}$  and  $i_{ac}$  are pure sinusoidal waveforms, i.e.,

$$\begin{cases} v_{ac} = V_{ac} \sin \omega t \\ i_{ac} = I_{ac} \sin \omega t \end{cases}, \quad (1)$$

where  $V_{ac}$  and  $I_{ac}$  are the amplitudes of  $v_{ac}$  and  $i_{ac}$ , respectively, and  $\omega$  is the line frequency. Then, the instantaneous input power  $p_{ac}$  is



$$p_{ac} = v_{ac} i_{ac} = \frac{V_{ac} I_{ac}}{E_{dc}} - \frac{V_{ac} I_{ac}}{E_{dc}} \cos(2\omega t). \quad (2)$$

$p_{ac}$  contains a double-line-frequency pulsating power  $p_r$  and a constant dc power  $P_{dc}$ . Assuming that  $p_r$  is fully buffered by  $C_b$ , the voltage and current of  $C_b$  can be further calculated as [22], [32]

$$v_c = \sqrt{\bar{V}_c^2 - \frac{P_{dc}}{\omega C_b} \sin(2\omega t)}, \quad (3)$$

$$i_c = -\frac{P_{dc} \cos(2\omega t)}{\sqrt{\bar{V}_c^2 - \frac{P_{dc}}{\omega C_b} \sin(2\omega t)}}, \quad (4)$$

where  $\bar{V}_c$  is the average voltage of  $v_c$  which is a design variable.

With the steady-state voltage and current expressions given in (1) – (4), the duty cycles of the active switches as well as the operating constraints of the rectifier can be obtained. Denote the durations of *State 1*–*State 4* in Fig. 4 as  $d_1 T_s$ ,  $d_2 T_s$ ,  $d_3 T_s$  and  $d_4 T_s$  respectively, where  $T_s$  is the switching period. Then,

$$d_1 + d_2 + d_3 + d_4 = 1. \quad (5)$$

From Table I, the duty cycles of the switches  $S_A$  and  $BS_B$  can be expressed as

$$d_A = d_1 + d_3, \quad (6)$$

$$d_B = d_1 + d_4. \quad (7)$$

Based on Fig. 4, the state-space-averaged line current  $i_{ac}$ , load current  $i_{dc}$  and capacitor current  $i_c$  over  $T_s$  can be calculated as (here, the averaging operator is omitted for simplicity)

$$|i_{ac}| = (d_1 + d_4) i_L = d_B i_L, \quad (8)$$

$$i_{dc} = i_L, \quad (9)$$

$$i_c = (d_4 - d_3)i_L = (d_B - d_A)i_L. \quad (10)$$

Equation (10) clearly indicates that  $i_c$  is positive (i.e.,  $C_b$  is charged) when  $d_3 < d_4$  (or  $d_A < d_B$ ), and vice versa, which is consistent with the observations made in Section II-B. Solution of (8)–(10) leads to

$$\begin{cases} d_A = \frac{|i_{ac}| - i_c}{i_L} = \frac{|i_{ac}| - i_c}{i_{dc}} \\ d_B = \frac{|i_{ac}|}{i_L} = \frac{|i_{ac}|}{i_{dc}} \end{cases}. \quad (11)$$

The duty cycles  $d_A$  and  $d_B$  in (11) must be within the range of 0–100%. Hence, the operating constraints of the proposed rectifier can be resolved as

$$\begin{cases} |i_{ac}| \leq i_{dc} + i_c \\ |i_{ac}| \geq i_c \\ |i_{ac}| \leq i_{dc} \end{cases}. \quad (12)$$

Solution of  $|i_{ac}| > i_c$  in (12) utilizing (1) and (4) suggests that

$$\bar{V}_c > \frac{V_{ac}}{2}. \quad (13)$$

Meanwhile, solution of  $|i_{ac}| < i_{dc}$  in (12) reveals that

$$V_{dc} \leq \frac{V_{ac}}{2}. \quad (14)$$

According to the energy conservation principle, equation (2) can be rearranged as

$$P_{ac}^{i_{ac}} = P_{dc}^{i_{dc}} + P_r^{i_c}. \quad (15)$$

By averaging (15) over a line period  $T_{line}$  while combining (8) and (9), one yields

$$\langle v_{dc} \rangle_{T_{line}} = \frac{\langle d_B |v_{ac}| i_L \rangle_{T_{line}}}{\langle i_L \rangle_{T_{line}}}, \quad (16)$$

where  $\langle \cdot \rangle_{T_{line}}$  is an averaging operator over  $T_{line}$ . Equation (16) indicates that the dc voltage conversion characteristics of the proposed rectifier have a similar form to that of the buck converter. Based on (14) and (16), the rectifier is capable of producing *any* output voltage lower than  $V_{ac}/2$  provided that (12) is satisfied.

#### D. Gate Signal Generation

According to (8)–(10),  $d_1$ ,  $d_2$ , and  $d_4$  can be expressed in terms of  $d_3$  as

$$\begin{cases} d_1 = \frac{|i_{ac}| - i_c}{i_{dc}} - d_3 \\ d_2 = \frac{i_{dc} - |i_{ac}|}{i_{dc}} - d_3 \\ d_4 = \frac{i_c}{i_{dc}} + d_3 \end{cases} \quad (17)$$

Equation (17) indicates that there is freedom in choosing  $d_3$ . If phase-shifted modulation (which is commonly adopted for controlling multilevel converters [14], [33]–[36] to boost the effective switching frequency) is adopted here, the active switching states are *State 1*, *State 3* and *State 4* when  $d_A + d_B \geq 1$ , while they become *State 2*, *State 3* and *State 4* when  $d_A + d_B < 1$  (see Fig. 5, where  $d_A$  and  $d_B$  are modulated using two out-of-phase triangular carriers, *Carrier\_a* and *Carrier\_b*, respectively). In both scenarios, the voltage across the inductor is switched between three voltage levels. Mathematically, Fig. 5 indicates that

$$\begin{cases} d_1 + d_3 + d_4 = 1 & (d_A + d_B \geq 1) \\ d_2 + d_3 + d_4 = 1 & (d_A + d_B < 1) \end{cases} \quad (18)$$

Combinations of (17) and (18) leads to  $d_1$ – $d_4$ , which can be expressed as

$$\begin{cases} d_1 = \frac{2|i_{ac}| - i_c - i_{dc}}{i_{dc}} \\ d_2 = 0 \\ d_3 = \frac{i_{dc} - |i_{ac}|}{i_{dc}} \\ d_4 = \frac{i_{dc} - |i_{ac}| + i_c}{i_{dc}} \end{cases} \quad (d_A + d_B \geq 1), \quad (19)$$

$$\begin{cases} d_1 = 0 \\ d_2 = \frac{i_{dc} - 2|i_{ac}| + i_c}{i_{dc}} \\ d_3 = \frac{|i_{ac}| - i_c}{i_{dc}} \\ d_4 = \frac{|i_{ac}|}{i_{dc}} \end{cases} \quad (d_A + d_B < 1). \quad (20)$$

In Fig. 6,  $d_1$ – $d_4$ ,  $d_A$  and  $d_B$  are plotted versus  $v_{ac}$ ,  $i_{ac}$ ,  $v_{dc}$  and  $v_c$  over one line period based on (1), (3), (4), (11), (19), (20) and the circuit specifications listed in Table IV. Fig. 6 shows that  $d_A$  and  $d_B$  are within 0–100%, indicating that the operating constraints are satisfied. Moreover, as  $d_A + d_B < 1$  throughout  $T_{line}$ ,  $d_1$  is always equal to zero in this specific design, i.e., switching *State 1* is deactivated.

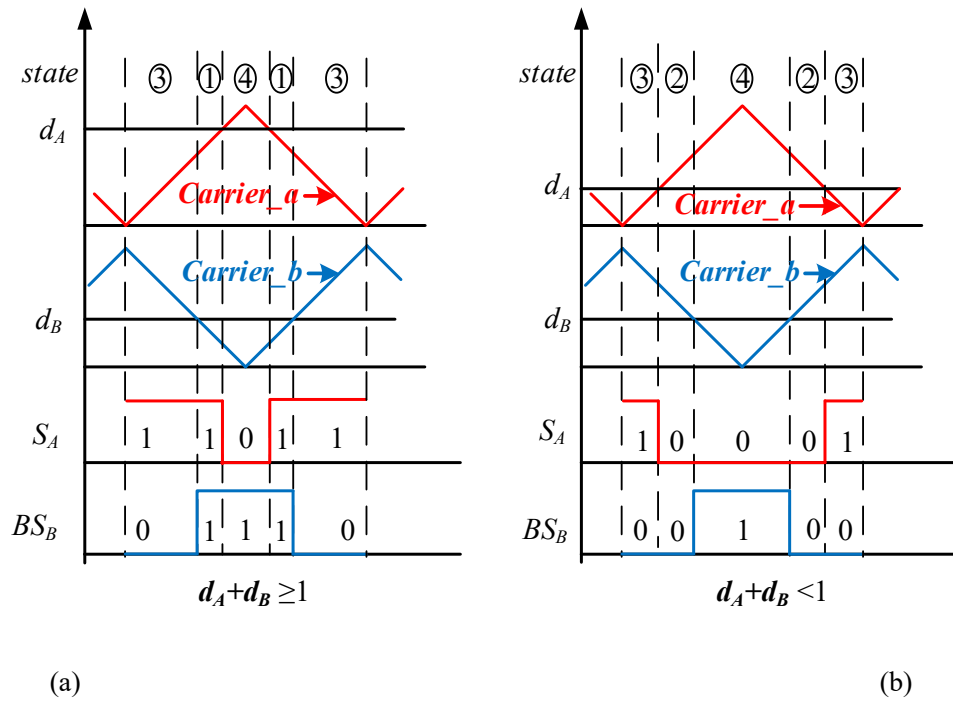


Fig. 5. Gate signal generated by two out-of-phase triangular carriers when (a)  $d_A + d_B \geq 1$  and (b)  $d_A + d_B < 1$ .

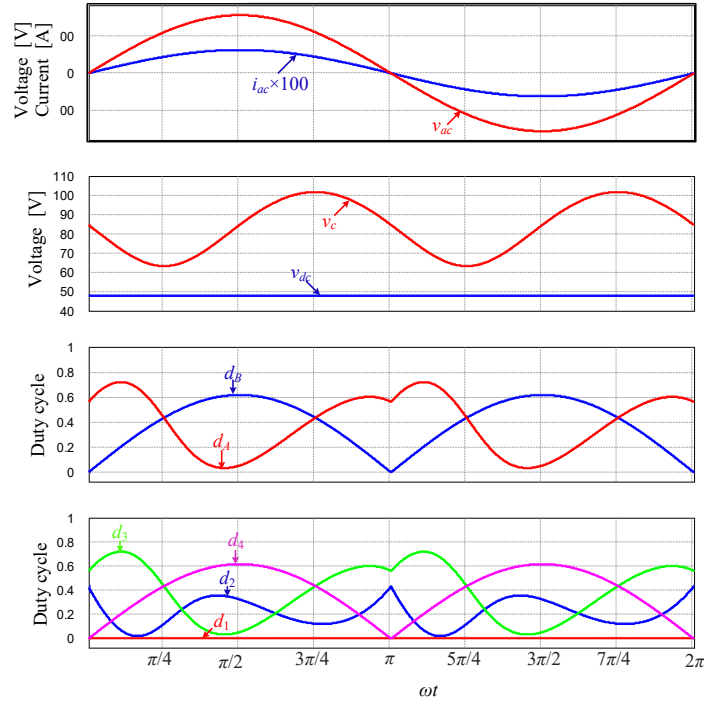


Fig. 6. Calculated  $v_{ac}$ ,  $i_{ac}$ ,  $v_{dc}$ ,  $v_c$ ,  $d_1$ – $d_4$ ,  $d_A$ , and  $d_B$  over one line period.

### III. ENHANCED AUTOMATIC POWER DECOUPLING CONTROL

Theoretically,  $d_A$  and  $d_B$  can be calculated based on (11) for open-loop control of the rectifier. However, the derivation of (11) does not take into consideration the power losses, nonlinearities and component tolerances which are non-negligible in practical design. Thus, a closed-loop controller must be developed to complement the system's operation. Here, a nonlinear closed-loop control method based on Enhanced Automatic-Power-Decoupling (E-APD) control is adopted [37], [38]. The design procedures of the controller are described as follows.

From Fig. 4, the state-space-averaged equations of the proposed rectifier can be obtained as

$$\begin{cases} L \frac{di_L}{dt} = (d_A - d_B)v_c + d_B |v_{ac}| - v_{dc} \\ C_{dc} \frac{dv_{dc}}{dt} = -\frac{v_{dc}}{R_{dc}} + i_L \\ C_b \frac{dv_c}{dt} = (d_B - d_A)i_L \end{cases} \quad (21)$$

Meanwhile, with reference to APD control strategy, the control outputs are selected as

$$\begin{cases} y_1 = Li_L \\ y_2 = i_{ac} = d_B i_L \end{cases}, \quad (22)$$

which represents the dc-port and ac-port dynamics, respectively [37].

Equations (21) indicates that the system is highly coupled (between the system states and the control inputs  $d_A$  and  $d_B$ ) and highly nonlinear (due to the multiplying operation of the control inputs and the system states). By differentiating the first equation of (22) with time, one has

$$\begin{cases} \dot{y}_1 = (d_A - d_B)v_c + d_B |v_{ac}| - v_{dc} \\ y_2 = i_{ac} = d_B i_L \end{cases} \quad (23)$$

If two new control inputs  $u_A$  and  $u_B$  are introduced such that

$$\begin{cases} y_1 = u_A \\ y_2 = u_B \end{cases}, \quad (24)$$

the original coupled and nonlinear system is now numerically transformed into two decoupled and linear subsystems. By solving (23) and (24), the feedback-linearization-decoupling law to convert the new control inputs back to the original control inputs can be derived as

$$\begin{cases} d_A = \frac{u_A + v_{dc} - \frac{u_B}{i_L} |v_{ac}|}{v_c} + \frac{u_B}{i_L} \\ d_B = \frac{u_B}{i_L} \end{cases} \quad (25)$$

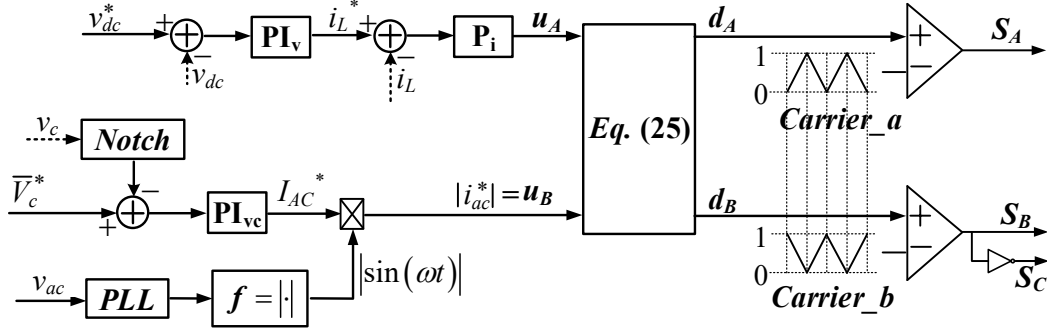


Fig. 7. Overall control diagrams of the employed enhanced automatic-power-decoupling control.

With reference to (24), the control of the rectifier can be achieved using simple linear controllers. As shown in Fig. 7,  $u_A$  is obtained using a proportional controller  $P_i$ , while  $u_B$  is directly derived from  $|i_{ac}^*|$  based on (22). Once  $u_A$  and  $u_B$  are known,  $d_A$  and  $d_B$  can be calculated using (25) for generating gate driving signals. In Fig. 7, the reference signal  $i_L^*$  is obtained from an outer voltage loop regulating  $v_{dc}$  at  $v_{dc}^*$ , while  $|i_{ac}^*|$  is derived from a second voltage loop regulating  $\bar{V}_c$  at  $\bar{V}_c^*$ . Here, a notch filter with a stopping band at the double-line frequency is employed to extract  $\bar{V}_c$ . The design of the PI controllers for the two voltage regulation loops and that of the P controller for the current regulation loop follow that of a conventional linear controller and are not detailed here [37].

#### IV. DESIGN CONSIDERATIONS

##### A. Active Switches and Diodes Design

Table II. Voltage stresses and maximum voltage stress for  $S_A$ ,  $D_A$ ,  $S_B$ ,  $D_B$ ,  $S_C$  and  $D_C$ .

Operating State	$S_A$	$D_A$	$BS_B$		$BS_C$	
State 1	0	$v_c$	0		$ v_{ac}  - v_c$	
State 2	$v_c$	0	$ v_{ac}  - v_c$		0	
State 3	0	$v_c$	$ v_{ac}  - v_c$		0	
State 4	$v_c$	0	0		$ v_{ac}  - v_c$	
Minimum voltage rating	$V_A$	$V_A$	$S_B$	$D_B$	$S_C$	$D_C$
			$V_{B+}$	$V_{B-}$	$V_{B-}$	$V_{B+}$

Table II summarizes the voltages across each power device during *State 1*–*State 4*. It is evident that the minimum voltage ratings of  $S_A$  and  $D_A$  (i.e.,  $V_A$ ) are the peak voltage of  $v_c$ . From (3),  $V_A$  can be expressed as

$$V_A = \max_{0 \leq t \leq T_{line}} \{v_c\} = \sqrt{\bar{V}_c^2 + \frac{P_{dc}}{\omega C_b}}, \quad (26)$$

which is highlighted in Fig. 8. On the other hand, Table II shows that the voltage stresses across the two bi-quadrant switches  $BS_B$  and  $BS_C$  are  $|v_{ac}| - v_c$  which is bipolar according to Fig. 8. Notice that  $S_C$  and  $D_B$  are ON when  $|v_{ac}| - v_c \geq 0$ . Thus, the minimum voltage ratings of  $S_B$  and  $D_C$  (i.e.,  $V_{B+}$ ) are

$$V_{B+} = \max_{0 \leq t \leq T_{line}} \{|v_{ac}| - v_c\} = \max_{0 \leq t \leq T_{line}} \left\{ |V_{ac} \sin \omega t| - \sqrt{\bar{V}_c^2 - \frac{P_{dc}}{\omega C_b}} \sin(2\omega t) \right\}. \quad (27)$$

Similarly, when  $|v_{ac}| - v_c < 0$ ,  $S_B$  and  $D_C$  are ON. The minimum voltage ratings of  $S_C$  and  $D_B$  (i.e.,  $V_{B-}$ ) then equal to

$$V_{B-} = \max_{0 \leq t \leq T_{line}} \{v_c - |v_{ac}|\} = \max_{0 \leq t \leq T_{line}} \left\{ \sqrt{\bar{V}_c^2 - \frac{P_{dc}}{\omega C_b}} \sin(2\omega t) - |V_{ac} \sin \omega t| \right\} = \bar{V}_c. \quad (28)$$



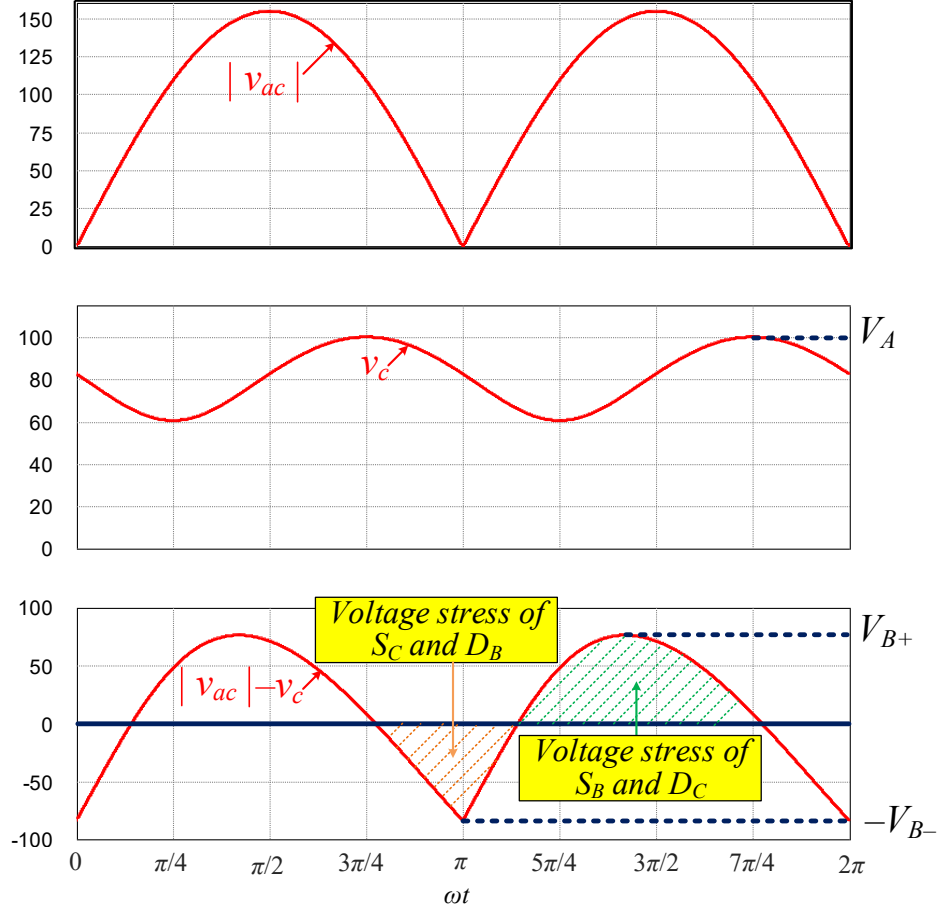


Fig. 8. Illustration of voltage stresses of all power devices during line period.

With the aid of (26)–(28),  $V_A$ ,  $V_{B+}$  and  $V_{B-}$  can be plotted against the output power and the flying capacitance used. The results are shown in Fig. 9(a) and (b) and are compared against  $V_{ac}$ , where  $V_{ac} = 110\sqrt{2}$  V,  $V_{dc} = 48$  V, and  $\bar{V}_c = 83$  V. According to Fig. 9, the following key observations can be made:

- (1) In Fig. 9(a),  $V_A$  and  $V_{B+}$  scale monotonically with  $P_{dc}$ , while  $V_{B-}$  is constant and equals to  $\bar{V}_c$ . The increase of  $V_A$  and  $V_{B+}$  with  $P_{dc}$  is due to the increased voltage ripple  $\Delta v_c$  as  $P_{dc}$  increases. Consequently,  $V_A$  and  $V_{B+}$  should be designed at full power;
- (2) In Fig. 9(b),  $V_A$  and  $V_{B+}$  decreases with the increase of  $C_b$  for a constant  $P_{dc}$ , while  $V_{B-}$  still equals to  $\bar{V}_c$ . Again, the decrease of  $V_A$  and  $V_{B+}$  is simply due to a smaller  $\Delta v_c$  when a larger  $C_b$  is employed;

(3) In this particular design where  $\bar{V}_c$  is selected closed to half of  $V_{ac}$  (i.e.,  $\bar{V}_c = 0.53 V_{ac}$ ),  $V_A$ ,  $V_{B+}$  and  $V_{B-}$  are also found to be closed to half of  $V_{ac}$  for a wide range of  $P_{dc}$  and  $C_b$ . In contrast, the voltage stresses of all power devices in the conventional buck PFC rectifier are  $V_{ac}$ . That is, the voltage stresses in the proposed rectifier are almost halved as compared to that of the conventional buck PFC rectifier.

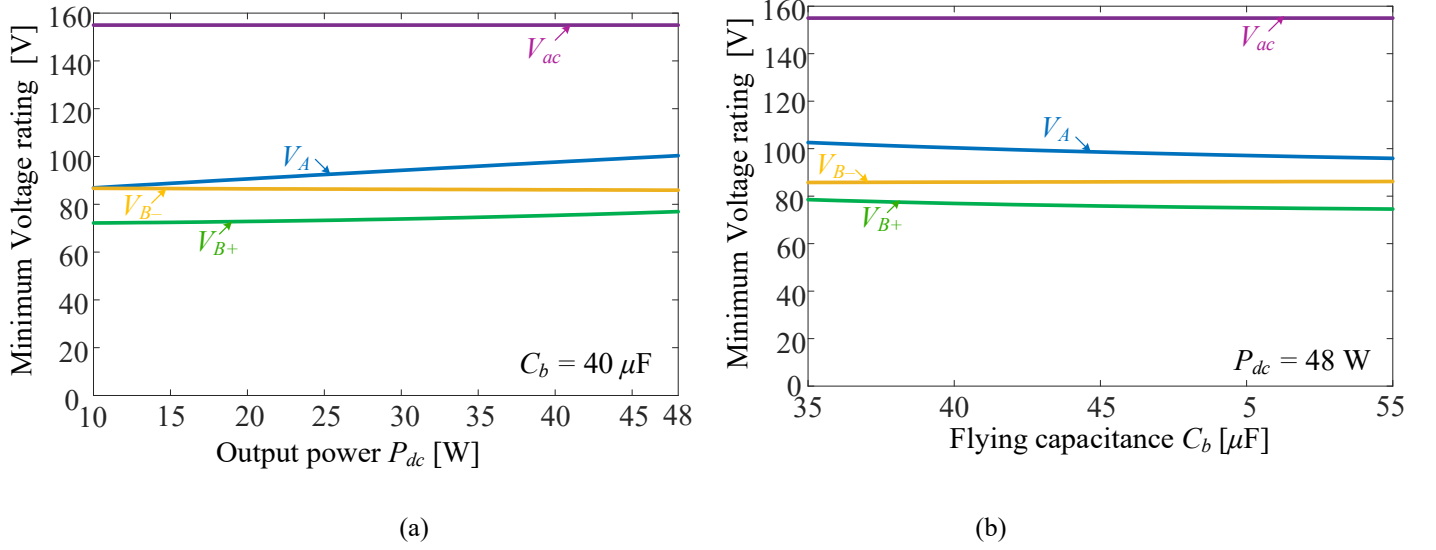


Fig. 9. The minimum voltage stresses versus (a) output power and (b) flying capacitance.

On the other hand, as the inductor current  $i_L$  flows through each switching component according to Fig. 4, the minimum current ratings  $I_{stress}$  for all the switching devices are identical and equal to the peak of  $i_L$ , i.e.,

$$I_{stress} = \max_{0 \leq t \leq T_{line}} \{i_L\} = \frac{V_{dc}}{R_{dc}} + \frac{\Delta i_{L\_rated}}{2}, \quad (29)$$

where  $\Delta i_{L\_rated}$  is the rated high-frequency inductor current ripple which will be designed in Section IV-C.

### B. Flying Capacitor Design

The design of  $C_b$  is essentially a compromise between system's power density and the system's operating constraints. In particular,  $C_b$  should be minimized while satisfying the constraints of (12).

Combination of (1), (4) and (12) leads to the design constraints of  $C_b$  as:

$$C_b \geq \max \{C_{b1}, C_{b2}\}, \quad (30)$$

where

$$C_{b1} = \max_{\omega t \in \left(0, \frac{\pi}{4}\right)} \left( \frac{P_{dc} \sin(2\omega t)}{\omega \left( \bar{V}_c^2 - \left( \frac{\cos(2\omega t)}{\frac{1}{V_{dc}} - \frac{2}{V_{ac}} |\sin \omega t|} \right)^2 \right)} \right), \quad (31)$$

$$C_{b2} = \max_{\omega t \in \left(\frac{\pi}{4}, \frac{3\pi}{4}\right)} \left( \frac{P_{dc} \sin(2\omega t)}{\omega \left( \bar{V}_c^2 - \frac{V_{ac}^2 \cos^2(2\omega t)}{4 \sin^2 \omega t} \right)} \right), \quad (32)$$

Given  $P_{dc}=48$  W,  $V_{dc} = 48$  V, and  $V_{ac} = 110\sqrt{2}$  V, and  $\bar{V}_c = 83$  V, one has  $C_{b1} = 19.4 \mu\text{F}$ , and  $C_{b2} = 31.4 \mu\text{F}$ .

Therefore,  $C_b = 40 \mu\text{F}$  is selected in this design.

### C. Inductor Design

The inductor  $L$  should be designed such that (i) the rectifier operates in the CCM and (ii) the peak-to-peak switching-frequency inductor current ripple  $\Delta i_L$  is less than a pre-specified value  $\Delta i_{L\_rated}$ .

The CCM of operation requires that

$$\Delta i_L < 2i_L. \quad (33)$$

Therefore, to ensure a CCM of operation,  $\Delta i_{L\_rated}$  should follow

$$\Delta i_{L\_rated} < \frac{2V_{dc}}{R_{dc}}. \quad (34)$$

To satisfy design criteria (ii),  $\Delta i_L$  needs to be resolved.

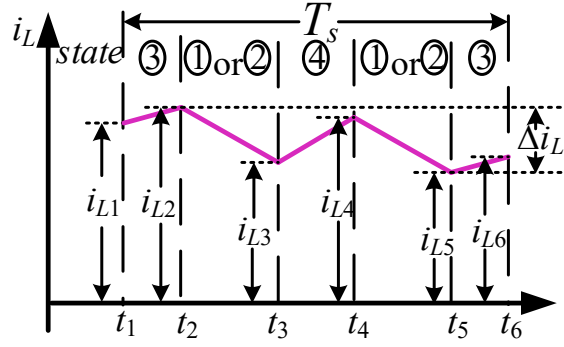


Fig. 10. Schematic diagram of the inductor current during one switching period.

The schematic waveform of  $i_L$  within one switching cycle  $T_s$  is depicted in Fig. 10. At time instances  $t_1$ – $t_6$ ,  $i_L$  reaches its local peak/valley with a value of  $i_{Ln}$ , respectively, where  $n \in \{1, 2, 3, 4, 5, 6\}$ , and

$$i_{L(m+1)} = i_{Lm} + \Delta i_{Lm}, \quad m \in \{1, 2, 3, 4, 5\}, \quad (35)$$

with  $\Delta i_{Lm}$  being the incremental inductor current during the interval from  $t_m$  to  $t_{m+1}$ . According to the annotated switching states in Fig. 10 and the corresponding inductor voltage in Table I,  $\Delta i_{Lm}$  can be derived as

$$\left\{ \begin{array}{l} \Delta i_{L1} = \frac{\gamma_1}{L} = \frac{d_3 T_s (v_c - v_{dc})}{2L} \\ \Delta i_{L2} = \frac{\gamma_2}{L} = \begin{cases} \frac{d_1 T_s (|v_{ac}| - v_{dc})}{2L} & (d_A + d_B \geq 1) \\ -\frac{d_2 T_s v_{dc}}{2L} & (d_A + d_B < 1) \end{cases} \\ \Delta i_{L3} = \frac{\gamma_3}{L} = \frac{d_4 T_s (|v_{ac}| - v_c - v_{dc})}{L} \\ \Delta i_{L4} = \frac{\gamma_4}{L} = \begin{cases} \frac{d_1 T_s (|v_{ac}| - v_{dc})}{2L} & (d_A + d_B \geq 1) \\ -\frac{d_2 T_s v_{dc}}{2L} & (d_A + d_B < 1) \end{cases} \\ \Delta i_{L5} = \frac{\gamma_5}{L} = \frac{d_3 T_s (v_c - v_{dc})}{2L} \end{array} \right. . \quad (36)$$

Therefore,  $\Delta i_L$  during the  $k$ th switching cycle is

$$\Delta i_L[k] = \max \{i_{L1}[k], L i_{L6}[k]\} - \min \{i_{L1}[k], L i_{L6}[k]\}, \quad (37)$$

which is a function of  $L$ . The minimum inductance  $L_{\min}$  can be obtained by equating the maximum  $\Delta i_L$  over  $T_{line}$  to  $\Delta i_{L\_rated}$ . With the aid of (1), (4), (19) and (20),  $L_{\min}$  is resolved as

$$L_{\min} = \frac{1}{\Delta i_{L\_rated}} \max_{k \in [1, T_{line}/T_s]} \left( \max \left\{ 0, \sum_{i=1}^{i=1} \gamma_i[k], L \sum_{i=1}^{i=5} \gamma_i[k] \right\} - \min \left\{ 0, \sum_{i=1}^{i=1} \gamma_i[k], L \sum_{i=1}^{i=5} \gamma_i[k] \right\} \right). \quad (38)$$

Fig. 11(a) and (b) illustrate the calculated  $L_{\min}$  against  $P_{dc}$  and  $V_{dc}$ , respectively. Here, a switching frequency of  $f_s = 50$  kHz,  $\Delta i_{L\_rated} = 0.6$  A,  $C_b = 40$   $\mu$ F,  $V_{ac} = 110\sqrt{2}$  V, and  $\bar{V}_c = 83$  V are utilized in the calculation. Fig. 11 shows that  $L_{\min}$  scales proportionally with  $P_{dc}$  and  $V_{dc}$ . Therefore,  $L_{\min}$  should be selected at the full power and the maximum  $V_{dc}$ . Based on Fig. 11,  $L_{min} = 0.965$  mH is needed for the 48-W/48-V system. Therefore,  $L = 1$  mH is selected in the final design.

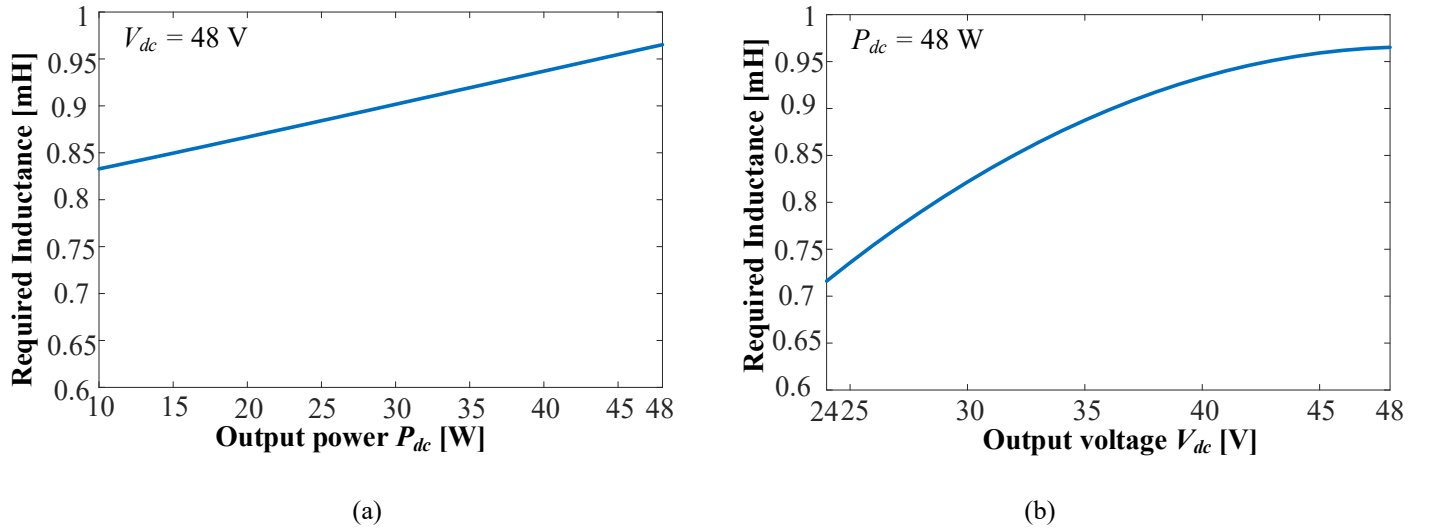


Fig. 11. The minimum inductance requirement for the proposed PFC rectifier versus (a) output power and (b) output voltage.

#### D. Comparison with Conventional Buck PFC Rectifier and PPB embeded Buck PFC Rectifiers

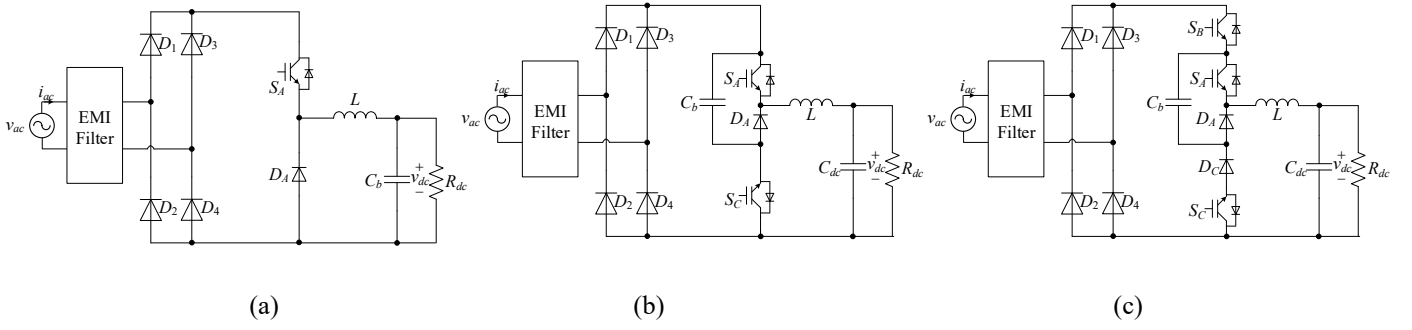


Fig. 12. Circuit diagrams of (a) conventional buck PFC rectifier, (b) the prior-art PPB embedded switching buck PFC rectifier in [26] and (c) the proposed three-level flying-capacitor buck PFC rectifier.

Referring to [39], the averaged line current  $i'_{ac}$  of the conventional buck PFC rectifier over  $T_s$  during half line period can be expressed as

$$i'_{ac} = \begin{cases} \frac{2\pi P_{dc} (\sin \omega t - \sin \theta_0)}{V_{ac} (\pi - 2\theta_0 + \sin 2\theta_0) - 4V_{dc} \cos \theta_0} & \omega t \in [\theta_0, \pi - \theta_0] \\ 0 & \omega t \in [0, \theta_0) \cup (\pi - \theta_0, \pi] \end{cases}, \quad (39)$$

where  $\theta_0 = \arcsin (V_{dc}/V_{ac})$ .

The averaged inductor current  $i'_L$  of the conventional buck PFC rectifier is [39]:

$$i'_L = \begin{cases} \frac{2\pi V_{ac} P_{dc} \sin \omega t (\sin \omega t - \sin \theta_0)}{V_{ac} V_{dc} (\pi - 2\theta_0 + \sin 2\theta_0) - 4V_{dc}^2 \cos \theta_0} & \omega t \in [\theta_0, \pi - \theta_0] \\ 0 & \omega t \in [0, \theta_0) \cup (\pi - \theta_0, \pi] \end{cases}. \quad (40)$$

Based on (1), (9), (39) and (40), the line and the inductor currents of the conventional buck PFC rectifier, the prior-art and the proposed PFC rectifier are plotted and compared in Fig. 13. A further comparison regarding several key figure-of-merits is also made in Table III. These comparisons are conducted under identical operating conditions:  $f_{sw} = 50$  kHz,  $P_{dc} = 48$  W,  $V_{dc} = 48$  V,  $V_{ac} = 110\sqrt{2}$  V, and  $\Delta i_{L\_rated} = 0.6$  A. The average buffering capacitor voltage for the prior-art PFC rectifier in [26] is chosen as  $\bar{V}_c = 1.15V_{ac} = 180$  V, and

that for the proposed rectifier is  $\bar{V}_c = 0.53V_{ac} = 83 \text{ V}$ . The buffering capacitance of the conventional buck PFC rectifier is designed to achieve a 3% peak-to-peak dc voltage ripple.

The conventional buck PFC rectifier is used as benchmark in the comparison, and its parameters can be calculated as: buffer capacitance  $C_b = 1840 \mu\text{F}$ ; peak voltage of  $C_b$ ,  $v_{c\_peak} = 48 \text{ V}$ ; main inductance  $L = 1.1 \text{ mH}$ ; peak inductor current  $I_{peak} = 2.56 \text{ A}$ ; peak voltage stress of active switches for  $S_A$  and  $D_A$  are  $155 \text{ V}$ .

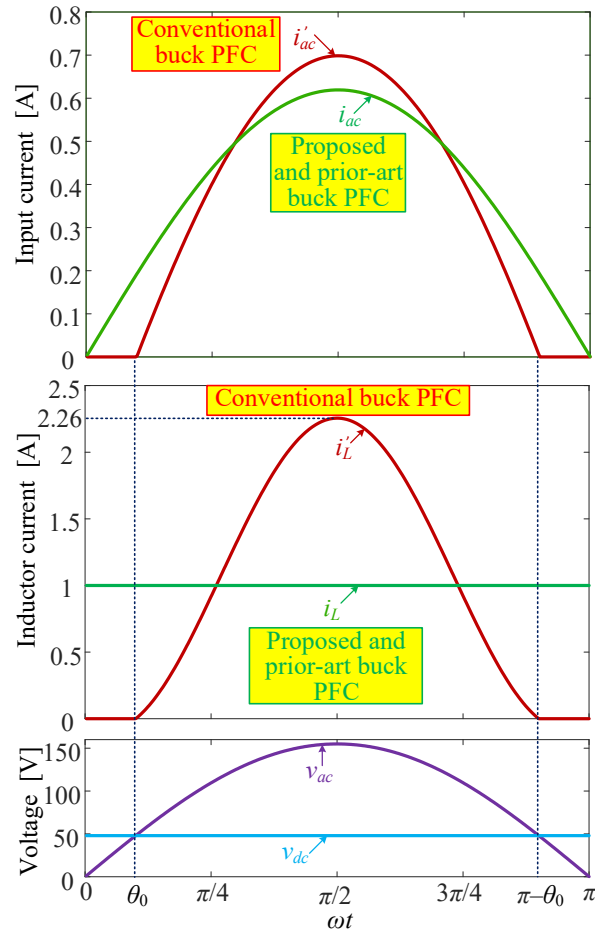


Fig. 13. Comparison of calculated ac input and inductor currents of the conventional and proposed buck PFC rectifiers.

Table III. Comparison of the three buck PFC rectifiers in Fig. 12 (Normalized by conventional buck PFC).

	Conventional buck PFC rectifier (Fig. 12 (a))	Prior-art PPB embedded switching buck PFC rectifier (Fig. 12 (b))	Proposed three-level buck PFC rectifier (Fig. 12c))
Unity power factor achievable	No	Yes	Yes
Power buffering method	Passive	Active	Active
Normalized energy storage requirement of $C_b$ , $0.5C_b V_{c\_peak}^2$ (p.u.)	1	0.34	0.094

Normalized energy storage requirement of $L$ , $0.5LI_{peak}^2$ (p.u.)	1	0.298	0.227
Normalized voltage stress of active switches (p.u.)	$S_A$ : 1	$S_A$ : 1.23 $S_C$ : 1.16	$S_A$ : 0.645 $S_B$ : 0.497 $S_C$ : 0.535
Normalized voltage stress of diodes (p.u.)	$D_A$ : 1	$D_A$ : 1.23	$D_A$ : 0.645 $D_C$ : 0.497
Normalized current stress (p.u.)	1	0.508	0.508

From Fig. 13 and Table III, the three rectifiers in Fig. 12 are compared in the following four aspects:

(i) Power factor and THD. The proposed rectifier and the prior-art rectifier have a pure sinusoidal line current resulting in higher power factor and lower THD compared with conventional PFC rectifier, of which the line current is discontinuous;

(ii) Volume of  $C_b$ . Table III shows that the energy storage requirement of  $C_b$  of the conventional buck PFC rectifier is relatively large, therefore electrolytic capacitors are typically adopted for  $C_b$ . For the prior-art and the proposed rectifiers, the energy storage requirements of  $C_b$  are reduced by 66% and 90.6%, respectively, as compared to that of the conventional buck PFC rectifier, leading to the viability of adopting non-electrolitic capacitors e.g. film or ceramic capacitors, in the circuit. As the volume of capacitor is directly proportional to its energy storage requirement  $0.5C_bV_c^2$ , the above results also indicate that the proposed rectifier can achieve a volume reduction of 72.4% in  $C_b$  as compared with the prior-art PFC rectifier, assuming an identical dielectric material for the non-electrolitic capacitors;

(iii) Volume of  $L$ . The core volume of an inductor is directly proportional to the energy storage requirement  $0.5LI_{peak}^2$ , assuming the same core permeability and maximum operating flux density. Table III suggests that the proposed rectifier can achieve a core volume reduction of 77% and 23.4%, respectively, as compared with the conventional and the prior-art PFC rectifiers, respectively;



(iv) Voltage and current stresses. Table III indicates that the voltage stresses of the active switches (i.e.,  $S_A$  and  $S_C$ ) of the prior-art PFC rectifier are of 23% and 16%, respectively, higher than that for  $S_A$  in the conventional buck PFC rectifier. On the other hand, a voltage stress reduction of 35.5%, 50.3%, and 46.5%, respectively for  $S_A$ ,  $S_B$ , and  $S_C$ , is achieved with the proposed rectifier than with the conventional buck PFC rectifier. Meanwhile, the current ratings for all switching devices of the prior-art and the proposed rectifiers are reduced by 49%, as compared to the conventional buck PFC rectifier, due to the reduction of the peak inductor current.

## V. EXPERIMENTAL VERIFICATION

Table IV. Key Experiment Parameters.

Parameters	Values	Parameters	Values
Input ac RMS voltage	110 V	Line frequency	60 Hz
output dc voltage $V_{dc}$	48 V	Switching frequency $f_s$	50 kHz
Full output power	48 W	Flying capacitor $C_b$	CKG57NX7T2E335M500JH $\times$ 20
Inductor $L$	2300LL-102	Output capacitor $C_{dc}$	CKG57KX7S2A156M335JH
$D_1$ – $D_4$ , $D_A$ and $D_C$	SBR10U200P5	$S_A$ – $S_C$	EPC2010C
Input EMI filter	2300LL-102 CKG57KX7T2J474M335JH		

A proof-of-concept 48-W prototype with the component specifications given in Table IV is constructed and tested as shown in Fig. 14. The design of the rectifier strictly follows that described in Section IV. The effect of capacitance derating of ceramic capacitors due to DC voltage bias are also considered [40]. Additionally, the front-end EMI filter is designed to have a cut-off frequency of 10 kHz to filter the switching-frequency harmonic current. The E-APD controller is implemented using a low-cost DSP (TMS320F28069). With a measured box dimension of 2.8 cm \* 4.3 cm \* 1.7 cm (1.09 in \* 1.68 in \* 0.66 in) and a total volume of 20.5 cm<sup>3</sup> (1.2 in<sup>3</sup>), the rectifier prototype achieves a power density of 2.34 W/cm<sup>3</sup> (40 W/in<sup>3</sup>) for the power stage of the converter.

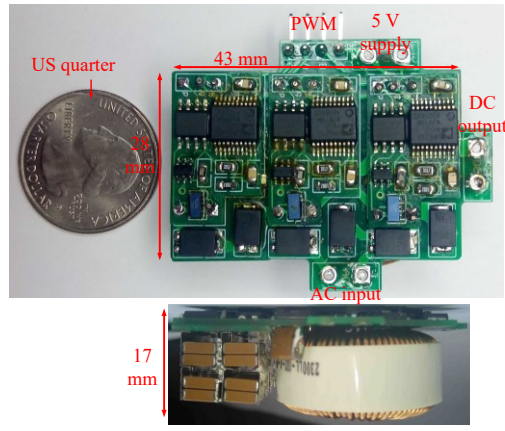
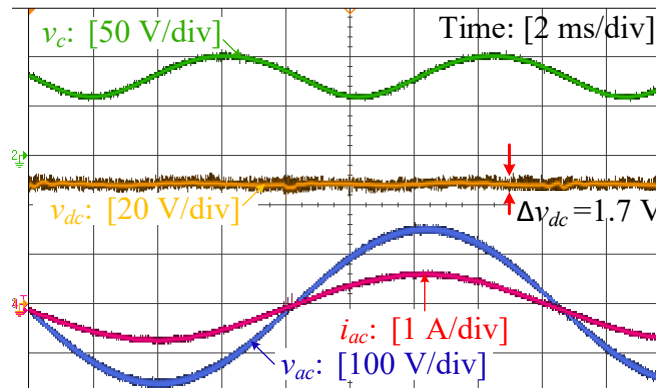


Fig. 14. Photograph of the experimental setup.

The steady-state waveforms of the proposed PFC rectifier at full load are shown in Fig. 15(a). It can be seen that unity power factor is achieved and that  $V_{dc}$  is well regulated at 48 V with negligible low-frequency voltage ripples (i.e., 3.5% of  $V_{dc}$ ). Meanwhile,  $v_c$  is pulsating significantly at a double-line frequency, indicating  $C_b$  is effectively buffering the pulsating ripple power. Fig. 15(b) and (c) further illustrate the voltage waveforms of all switching devices in comparison with  $v_{ac}$  and  $v_c$ . Fig. 15(b) clearly shows that the voltages across  $S_A$  and  $D_A$  are clamped by  $v_c$ . In Fig. 15(b), a differential voltage of  $|v_{ac}| - v_c$  is imposed on  $S_B$  and  $D_C$  when  $|v_{ac}| \geq v_c$ ; while a voltage of  $v_c - |v_{ac}|$  is imposed on  $S_C$  and the diode bridge when  $|v_{ac}| \leq v_c$ . The observations in Fig. 15(b) and (c) validated the reduced voltage stresses achievable with the proposed PFC rectifier.



(a)

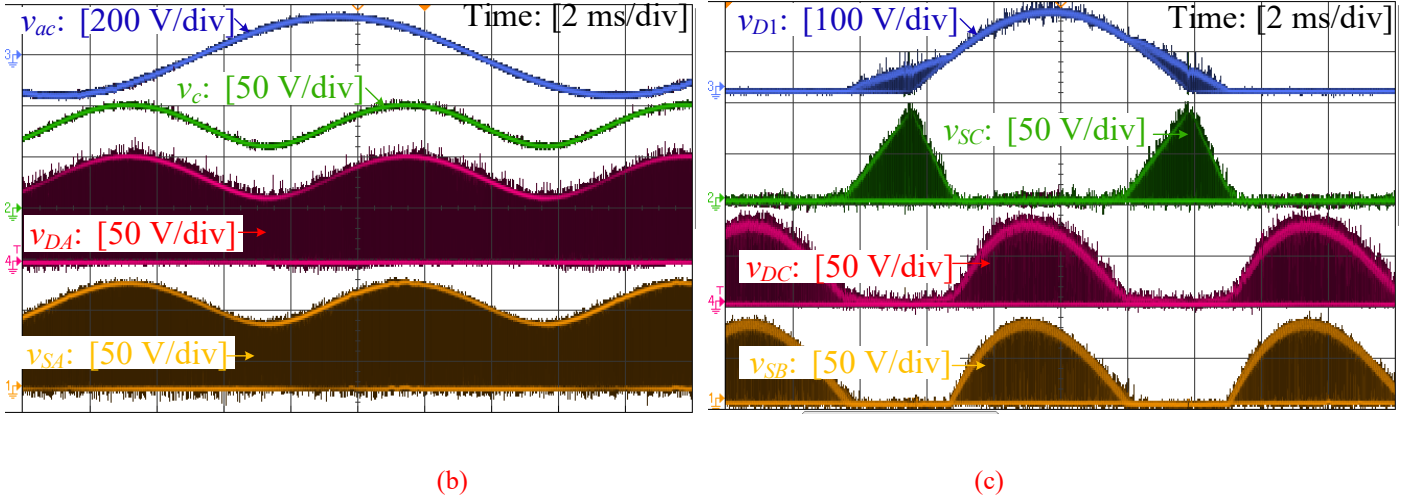


Fig. 15. Measured steady-state (a) waveforms of the proposed PFC rectifier; (b) voltage waveforms of  $S_A$ ,  $D_A$ ,  $C_b$  and ac input voltage; (c) voltage waveforms of  $S_B$ ,  $S_C$ ,  $D_C$ , and  $D_1$ .

The transient performance of the proposed rectifier are also tested and the waveforms are captured as shown in Fig. 16 (a) and (b). In Fig. 16 (a), the load is step changed between 28 W and 48 W. With the proposed E-APD controller,  $v_{dc}$  is almost immune to both step-up and -down load change. A step change of the load leads to a step change of the ripple power between the ac input and the dc output. Due to the robustness of the E-APD control strategy, the ripple power is automatically transferred to  $C_b$ , resulting in a sudden voltage undershoot/overshoot of  $v_c$  subsequent to the transient interval. In Fig. 16 (b), a step change of the line voltage between 95 Vrms to 110 Vrms is conducted. Despite large line voltage variations,  $v_{dc}$  again retains tight voltage regulation and demonstrates strong robustness against the line voltage disturbances.

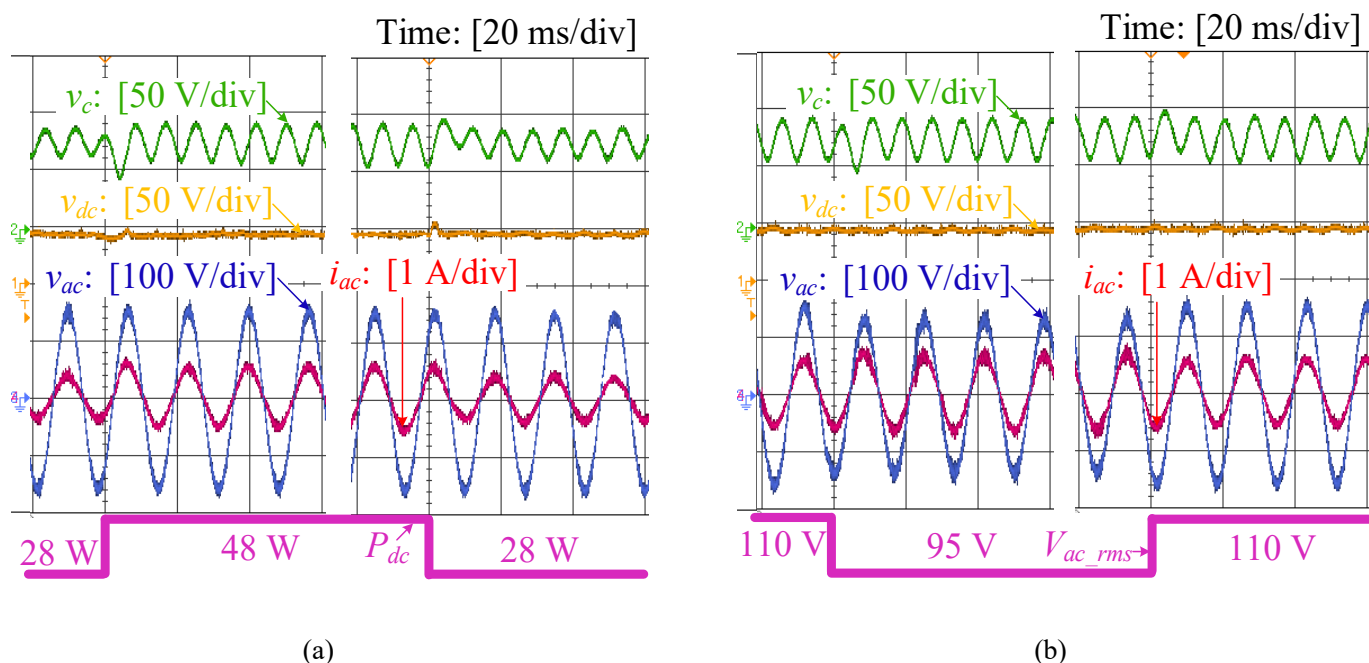
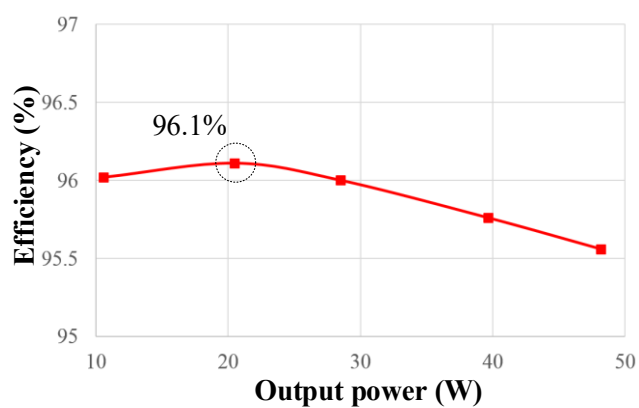
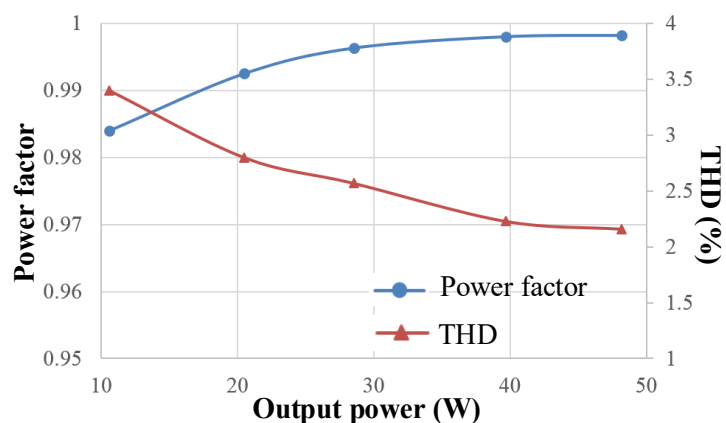


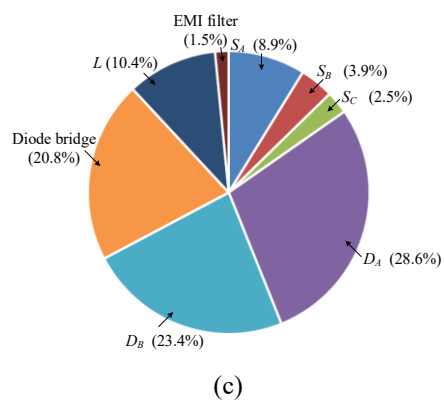
Fig. 16. Dynamic waveforms of the proposed rectifier in response to (a) a step change of the load and (b) a step change of the line voltage.



(a)



(b)



(c)

Fig. 17. Measured (a) efficiency, (b) input power factor and THD of the proposed PFC rectifier versus the output power and (c) estimated loss breakdown.

Fig. 17(a) records the rectifier's power conversion efficiency from 10 W to 48 W. The rectifier reaches a peak efficiency of 96.1%. Overall, the efficiency curve is fairly flat over a wide load range. The power factor and the THD of the proposed rectifier are also measured and shown in Fig. 17(b). A power factor of 0.998 and a THD of 2.2% are achieved when the rectifier operates at full load 48 W. Finally, an estimated power loss breakdown is illustrated in Fig. 17 (c) at full load (i.e., 48 W). The results show that the major losses of the rectifier are the diodes' conduction and reverse recovery losses (72.8%).

## CONCLUSIONS

In this paper, a three-level flying-capacitor buck PFC rectifier without electrolytic capacitor is proposed. By exploiting the switching states of the conventional three-level flying-capacitor converter, we are able to embed active pulsating-power-buffering function into the operation of the converter. The proposed solution is found to have lower voltage/current stresses, reduced magnetic and capacitive footprint, as well as a higher PF and a lower THD, as compared to those of a conventional buck PFC converter. Despite the use of a slighted complicated nonlinear controller, the proposed solution demonstrates strong robustness against load and line voltage disturbances while the power conversion efficiency remains higher than 95.5% for a wide load range. The proposed solution extends the existing single-phase PFC rectifier families which has an active PPB function, and may lead to new circuit topologies towards achieving  $H^3$  single-phase power conversion.

## REFERENCES

- [1] M. Rico-secades, A. J. Calleja, J. Ribas, E. L. Corominas, J. M. Alonso, J. Cardesín, and J. García-garcía, "Evaluation of a low-cost permanent emergency lighting system based on high-efficiency LEDs," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1386–1390, Sep. 2005.
- [2] P. S. Almeida, D. Camponogara, M. A. D. Costa, H. Braga, and J. M. Alonso, "Matching LED and driver life spans: a review of different techniques," *IEEE Ind. Electron. Mag.*, vol. 9, no. 2, pp. 36–47, Jun. 2015.
- [3] Y. Wang, J. M. Alonso, and X. Ruan, "A review of LED drivers and related technologies," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5754–5765, Jul. 2017.

- [4] Y. C. Li and C. L. Chen, "A novel single-stage high-power-factor AC-to-DC LED driving circuit with leakage inductance energy recycling," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 793–802, Feb. 2012.
- [5] J. M. Alonso, J. Viña, D. G. Vaquero, G. Martínez, and R. Osorio, "Analysis and design of the integrated double Buck – Boost converter as a high-power-factor driver for power-LED lamps," *IEEE Trans. Ind. Electron.*, vol. 59, no. 4, pp. 1689–1697, Apr. 2012.
- [6] S. Li, S. C. Tan, C. K. Lee, E. Waffenschmidt, S. Y. R. Hui, and C. K. Tse, "A survey, classification, and critical review of light-emitting diode drivers," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1503–1516, Feb. 2016.
- [7] S. Lim, S. Bandyopadhyay, and D. J. Perreault, "High-frequency isolated ac-dc converter with stacked architecture," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2017, pp. 1789–1796.
- [8] Y. C. Li, F. C. Lee, Q. Li, X. Huang, and Z. Liu, "A novel AC-to-DC adaptor with ultra-high power density and efficiency," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2016, vol. 2016–May, pp. 1853–1860.
- [9] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-based MHz totem-pole PFC rectifier," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 799–807, Sep. 2016.
- [10] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep. 2005.
- [11] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.
- [12] M. A. Vitorino, L. F. S. Alves, R. Wang, and M. B. De Rossiter Correa, "Low-frequency power decoupling in single-phase applications: a comprehensive overview," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2892–2912, Apr. 2017.
- [13] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.
- [14] H. Watanabe, T. Sakuraba, K. Furukawa, K. Kusaka, and J. Itoh, "Development of DC to single-phase AC voltage source inverter with active power decoupling based on flying-capacitor DC/DC converter," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4992–5004, Jun. 2018.
- [15] L. Han and N. Narendran, "An accelerated test method for predicting the useful life of an LED driver," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2249–2257, Aug. 2011.
- [16] J. W. Kolar, D. Bortis, and D. Neumayr, "The ideal switch is not enough," *Proc. Int. Symp. Power Semicond. Devices ICs*, vol. 2016–July, pp. 15–22, 2016.
- [17] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters—an overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep. 2014.
- [18] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara, "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430–1443, May 2011.
- [19] S. Wang, X. Ruan, K. Yao, S. C. Tan, Y. Yang, and Z. Ye, "A flicker-free electrolytic capacitor-less AC-DC LED driver," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4540–4548, Nov. 2012.
- [20] H. Wang, H. S. H. Chung, and W. Liu, "Use of a series voltage compensator for reduction of the dc-link capacitance in a capacitor-supported system," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1163–1175, Mar. 2014.
- [21] S. Qin, Y. Lei, C. Barth, W. C. Liu, and R. C. N. Pilawa-Podgurski, "A high power density series-stacked energy buffer for power pulsation decoupling in single-phase converters," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4905–4924, Jun. 2017.
- [22] W. Qi, H. Wang, X. Tan, G. Wang, and K. D. T. Ngo, "A novel active power decoupling single-phase PWM rectifier topology," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2014, pp. 89–95.
- [23] S. Li, W. Qi, S. C. Tan, and S. Y. R. Hui, "Integration of an active filter and a single-phase AC/DC converter with reduced capacitance requirement and component count," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4121–4137, Jun. 2016.
- [24] Q. C. Zhong, W. L. Ming, W. Sheng, and Y. Zhao, "Beijing converters: bridge converters with a capacitor added to reduce leakage currents, DC-bus voltage ripples, and total capacitance required," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 325–335, Jan. 2017.
- [25] Y. Tang and F. Blaabjerg, "A component-minimized single-phase active power decoupling circuit with reduced current stress to semiconductor switches," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2905–2910, Jun. 2015.
- [26] Y. Ohnuma and J. I. Itoh, "A novel single-phase buck PFC AC-DC converter with power decoupling capability using an active buffer," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1905–1914, May 2014.
- [27] S. Li, W. Qi, S. C. Tan, and S. Y. R. Hui, "A single-stage two-switch PFC rectifier with wide output voltage range and automatic AC ripple power decoupling," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6971–6982, Sep. 2017.
- [28] Y. Liu, Y. Sun, M. Su, and F. Liu, "Control method for the Sheppard – Taylor PFC rectifier to reduce capacitance requirements," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2714–2722, Mar. 2018.
- [29] Y. Liu, Y. Sun, and M. Su, "A control method for bridgeless Cuk/SePIC PFC rectifier to achieve power decoupling," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 7272–7276, Sep. 2017.

- [30] W. Qi, S. Li, S. C. Tan, and S. Y. Hui, "A single-phase three-level flying-capacitor PFC rectifier without electrolytic capacitors," *IEEE Trans. Power Electron.*, 2018.
- [31] J. A. Cobos, H. Cristbal, D. Serrano, R. Ramos, J. A. Oliver, and P. Alou, "Differential power as a metric to optimize power converters and architectures," *2017 IEEE Energy Convers. Congr. Expo. ECCE 2017*, vol. 2017-Janua, no. c, pp. 2168–2175, 2017.
- [32] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.
- [33] T. A. Meynard, M. Fadel, and N. Aouda, "Modeling of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 44, no. 3, pp. 356–364, Jun. 1997.
- [34] Y. Lei, C. Barth, S. Qin, W.-C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2-kW single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8570–8581, Nov. 2017.
- [35] A. Stillwell, C. N. Robert, and Pilawa-Podgurski, "A 5-level flying capacitor multi-level converter with integrated auxiliary power supply and start-up," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 8993, no. c, pp. 2932–2938, 2017.
- [36] Z. Liao, Y. Lei, and R. C. N. Pilawa-Podgurski, "Analysis and design of a high power density flying-capacitor multilevel boost converter for high step-up conversion," *IEEE Trans. Power Electron.*, vol. 8993, no. c, 2018.
- [37] S. Li, W. Qi, S. C. Tan, and S. Y. Hui, "Enhanced automatic-power-decoupling control method for single-phase AC-to-DC converters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1816–1828, Feb. 2018.
- [38] H. Yuan, S. Li, W. Qi, S. C. Tan, and R. Hui, "On nonlinear control of single-phase converters with active power decoupling function," *IEEE Trans. Power Electron.*, 2018.
- [39] L. Huber, L. Gang, and M. M. Jovanović, "Design-oriented analysis and performance evaluation of buck PFC front end," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 85–94, Jan. 2010.
- [40] C. Barth, T. Foulkes, I. Moon, Y. Lei, S. Qin, and R. C. N. Pilawa-Podgurski, "Experimental evaluation of capacitors for power buffering in single-phase power converters," *IEEE Trans. Power Electron.*, vol. 8993, no. c, pp. 1–1, 2018.